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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,096	07/23/2003	Seung-Jae Lee	2522-022	9000
20575	7590	08/09/2005	EXAMINER	
MARGER JOHNSON & MCCOLLOM, P.C. 210 SW MORRISON STREET, SUITE 400 PORTLAND, OR 97204			VU, DAVID	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.		Applicant(s)	
	10/626,096		LEE ET AL.	
	Examiner		Art Unit	
	DAVID VU		2818	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06/15/05.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 13-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8 is/are allowed.
- 6) ☒ Claim(s) 1-7, 9-11 and 13-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>06/15/05</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### **Claim Rejections - 35 USC § 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-4 are rejected under 35 U. S. C. 102(b) as being anticipated by Nakano Atsushi (JP 6-140355).

Regarding claims 1 and 4, Nakano Atsushi (See CONSTITUTION) disclose a method for forming an electrode, comprising: forming a polysilicon layer 3 on a semiconductor substrate; forming an amorphous silicon capping layer 4 on the polysilicon layer 3; and depositing a silicide layer 5 on the capping layer.

2. Claims 1-4 and 10-16 are rejected under 35 U. S. C. 102(b) as being anticipated by Chang et al. (US Pat. 6,180,454, herein after Chang).

Regarding claims 1 and 4, Chang (See ABSTRACT) disclose a method for forming an electrode, comprising: forming a polysilicon layer (second poly layer/poly 2/control gate) on a semiconductor substrate; forming an amorphous silicon capping layer on the polysilicon layer (col. 5, lines 34-36); and depositing a silicide layer on the capping layer (col. 6, lines 6-13). Note that the term poly 2 includes both amorphous silicon and polysilicon layers (col. 5, lines 34-36).

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Regarding claims 10, 12 and 15, Chang (See ABSTRACT) disclose a semiconductor memory device, comprising: a gate oxide layer formed on a semiconductor substrate; a floating gate electrode (first poly layer) formed on the gate oxide layer; an intergate dielectric layer (insulating layer/ONO) formed on the floating gate electrode; a polysilicon layer (second poly layer/poly 2/control gate) on a semiconductor substrate; an amorphous silicon capping layer on the polysilicon layer (col. 5, lines 34-36); and a silicide layer on the capping layer (col. 6, lines 6-13). Note that the term poly 2 includes both amorphous silicon and polysilicon layers (col. 5, lines 34-36).

Regarding claims 2, 3, 11, 14 and 16, Chang disclose the silicide layer (tungsten silicide) is formed using a dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas (col. 6, lines 6-13), and wherein the capping layer (poly 2) is formed to have a thickness from about 1000-1400Å (sufficient to prevent chlorine ions dissociated from the dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas from diffusing toward the polysilicon layer) (col. 6, lines 2-3)

Regarding the limitation "wherein the polysilicon layer is formed by crystallizing amorphous silicon" (claim 13) or "wherein the tungsten silicide layer is formed using dichlorosilane" (claim 15), such limitation does not further define the structure as instantly claimed, nor serve to distinguish over Hasegawa. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se

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which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw make clear.

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 5-7 and 9 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang (US Pat. 6,180,454) in view of Oka et al. (US Pat. 6,235,563, herein after Oka)

Regarding claims 5 and 9, Chang (See ABSTRACT) disclose a flash memory device involving the steps of forming a gate oxide layer formed on a semiconductor substrate; a floating gate electrode (first poly layer) formed on the gate oxide layer; an intergate dielectric layer (insulating layer/ONO) formed on the floating gate electrode; a polysilicon layer (second poly layer/poly 2/control gate) on a semiconductor substrate; an amorphous silicon capping layer on the polysilicon layer (col. 5, lines 34-36); and a silicide layer on the capping layer (col. 6, lines 6-13). Note that the term poly 2 includes both amorphous silicon and polysilicon layers (col. 5, lines 34-36).

Chang fails to disclose the polysilicon layer of the control gate (poly 2) is formed by an amorphous silicon layer then annealing the amorphous silicon layer to form a polysilicon layer. However, Oka teaches a polycrystalline film (polysilicon) with high purity has been obtained by performing solid phase recrystallization on an amorphous silicon film formed by annealing the amorphous silicon film in a nitrogen atmosphere (See ABSTRACT). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the annealing process of Oka in the method of Chang, because it would have provided the advantageous /benefit of forming a polycrystalline thin films having high polycrystalline quality, larger crystal grains and good crystal grain orientation.

Regarding claims 6 and 7, Chang disclose the silicide layer (tungsten silicide) is formed using a dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas (col. 6, lines 6-13), and wherein the capping layer (poly 2) is formed to have a thickness from about 1000-1400Å (col. 6, lines 2-3).

### **Allowable Subject Matter**

4. Claim 8 is allowed.

The following is an examiner's statement of reasons for allowance: the prior art of record, either singularly or in combination, does not disclose or suggest an Applicant's claimed method for fabricating a control gate electrode layer of a semiconductor device electrode the method comprising: forming an amorphous silicon capping layer on the polysilicon layer; and forming a tungsten silicide layer on the capping layer; wherein forming the tungsten silicide layer comprises: supplying a first silane ( $\text{SiH}_4$ ) gas to a process chamber in which a wafer including the thin film of amorphous silicon is loaded; supplying a dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas and a tungsten hexafluoride ( $\text{WF}_6$ ) gas to the process chamber to deposit the tungsten silicide layer on the capping layer; purging the dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) gas and the tungsten hexafluoride ( $\text{WF}_6$ ) gas from the process chamber; and supplying a second silane ( $\text{SiH}_4$ ) gas to the process chamber.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."



### **Response to Arguments**

5. Applicant's arguments with respect to claims 1-7, 9-11 and 13-16 have been considered but are moot in view of the new ground(s) of rejection.

### **Conclusion**

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Vu

August 07, 2005.